

FAN7842

High and Low Side Gate Driver

Features

- Floating Channels Designed for Bootstrap Operation to +200V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at $V_{CC}=V_{BS}=15V$
- V_{CC} & V_{BS} Supply Range from 10V to 20V
- UVLO Functions for Both Channels
- TTL-Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50ns
- Output In-phase with Input Signal

Applications

- Half- and Full-Bridge Converters
- Current-Fed Push-Pull Converters
- Synchronous Buck Converters

Description

The FAN7842, a monolithic high and low side gate drive IC, which can drive MOSFETs and IGBTs that operate up to +200V.

Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of the high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_S=-9.8V$ (typical) for $V_{BS}=15V$. The input logic level is compatible with standard TTL-series logic gates.

The UVLO circuits for both channels prevent malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. Output driver current (source/sink) is typically 350mA/650mA, respectively.

8-SOP



Ordering Information

| Part Number | Operating Temp. Range | Pb-Free | Package | Packing Method |
|--------------------------|-----------------------|---------|---------|----------------|
| FAN7842M ⁽¹⁾ | -40°C to +125°C | Yes | 8-SOP | Tube |
| FAN7842MX ⁽¹⁾ | | | | Tape & Reel |

Note:

1. These devices passed wave soldering test by JESD22A-111.

Typical Application Diagrams

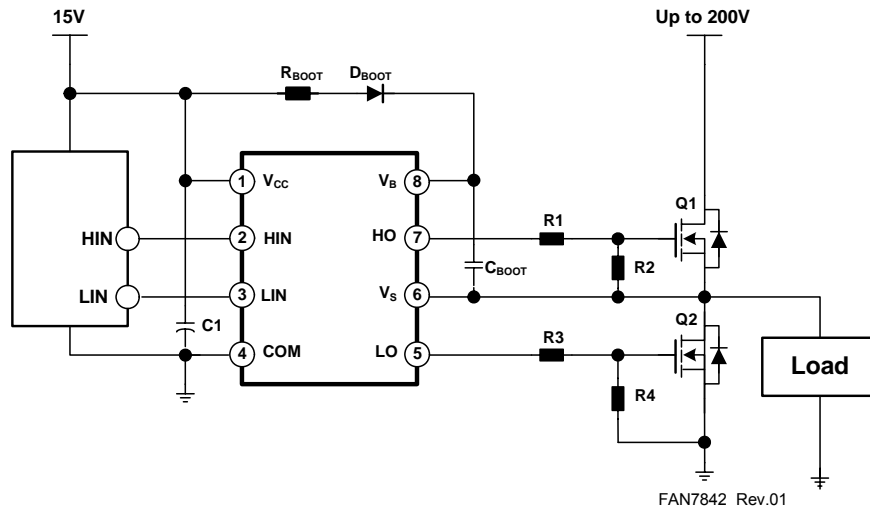


Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram

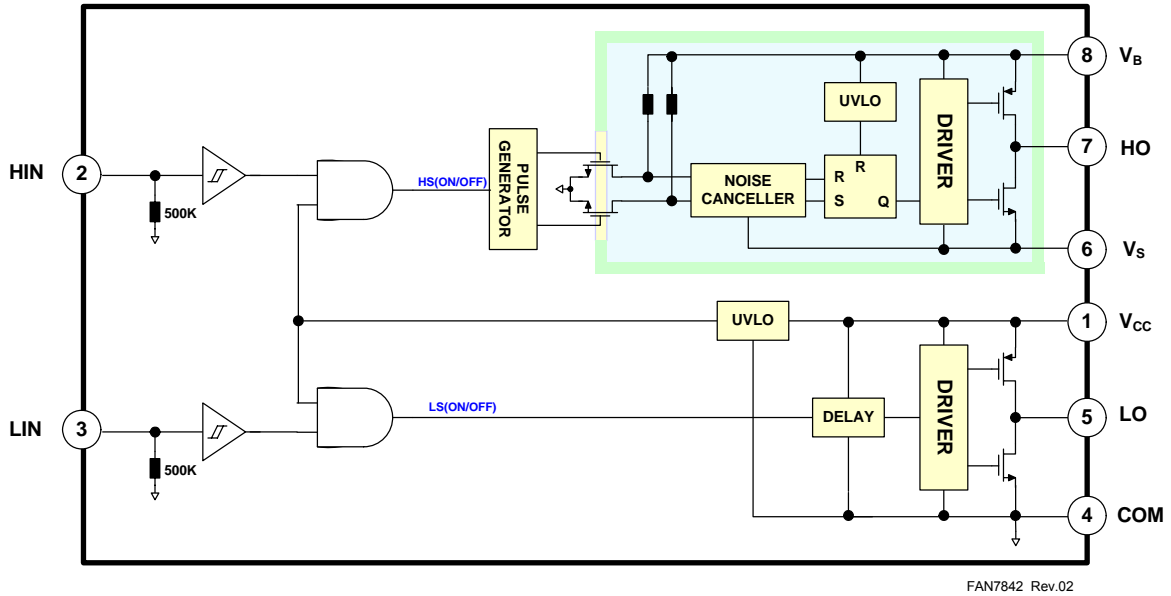
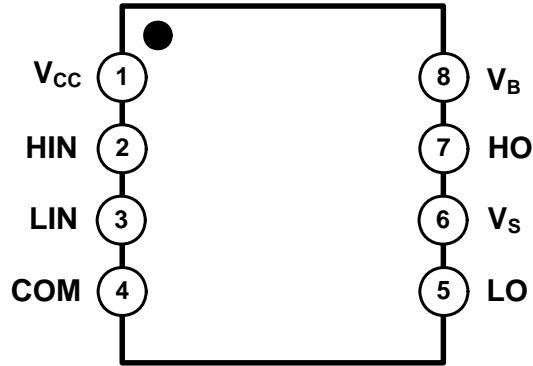


Figure 2. Functional Block Diagram

Pin Configuration



FAN7842 Rev.01

Figure 3. Pin Configuration (Top View)

Pin Definitions

| Pin # | Name | Description |
|-------|----------|--|
| 1 | V_{CC} | Low-Side Supply Voltage |
| 2 | HIN | Logic Input for High-Side Gate Driver Output |
| 3 | LIN | Logic Input for Low-Side Gate Driver Output |
| 4 | COM | Logic Ground and Low-Side Driver Return |
| 5 | LO | Low-Side Driver Output |
| 6 | V_S | High Voltage Floating Supply Return |
| 7 | HO | High-Side Driver Output |
| 8 | V_B | High-Side Floating Supply |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------|---|-------------|--------------|-----------------------------|
| V_S | High-side offset voltage | V_B-25 | $V_B+0.3$ | V |
| V_B | High-side floating supply voltage | -0.3 | 225 | |
| V_{HO} | High-side floating output voltage HO | $V_S-0.3$ | $V_B+0.3$ | |
| V_{CC} | Low-side and logic fixed supply voltage | -0.3 | 25 | |
| V_{LO} | Low-side output voltage LO | -0.3 | $V_{CC}+0.3$ | |
| V_{IN} | Logic input voltage (HIN, LIN) | -0.3 | $V_{CC}+0.3$ | |
| COM | Logic ground | $V_{CC}-25$ | $V_{CC}+0.3$ | |
| dVs/dt | Allowable offset voltage slew rate | | 50 | |
| $P_D^{(2)(3)(4)}$ | Power dissipation | | 0.625 | W |
| θ_{JA} | Thermal resistance, junction-to-ambient | | 200 | $^{\circ}\text{C}/\text{W}$ |
| T_J | Junction temperature | | 150 | $^{\circ}\text{C}$ |
| T_{STG} | Storage temperature | | 150 | $^{\circ}\text{C}$ |

Note:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
 - JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
 - JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- Do not exceed P_D under any circumstances.

Recommended Operating Ratings

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|----------|--|------------|----------|------|
| V_B | High-side floating supply voltage | V_S+10 | V_S+20 | V |
| V_S | High-side floating supply offset voltage | $6-V_{CC}$ | 200 | |
| V_{HO} | High-side (HO) output voltage | V_S | V_B | |
| V_{LO} | Low-side (LO) output voltage | COM | V_{CC} | |
| V_{IN} | Logic input voltage (HIN, LIN) | COM | V_{CC} | |
| V_{CC} | Low-side supply voltage | 10 | 20 | |
| T_A | Ambient temperature | -40 | 125 | |

Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15.0V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|----------------------------|---|---|------|------|------|---------|
| V_{CCUV+} V_{BSUV+} | V_{CC} and V_{BS} supply under voltage positive going threshold | | 8.2 | 9.2 | 10.0 | V |
| V_{CCUV-} V_{BSUV-} | V_{CC} and V_{BS} supply under voltage negative going threshold | | 7.6 | 8.7 | 9.6 | |
| V_{CCUVH} V_{BSUVH} | V_{CC} supply under voltage lockout hysteresis | | | 0.6 | | |
| I_{LK} | Offset supply leakage current | $V_B = V_S = 200V$ | | | 10 | μA |
| I_{QBS} | Quiescent V_{BS} supply current | $V_{IN} = 0V$ or 5V | | 45 | 120 | |
| I_{QCC} | Quiescent V_{CC} supply current | $V_{IN} = 0V$ or 5V | | 70 | 180 | |
| I_{PBS} | Operating V_{BS} supply current | $f_{IN} = 20kHz$, rms value | | | 600 | μA |
| I_{PCC} | Operating V_{CC} supply current | $f_{IN} = 20kHz$, rms value | | | 600 | |
| V_{IH} | Logic "1" input voltage | | 2.9 | | | V |
| V_{IL} | Logic "0" input voltage | | | | 0.8 | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | $I_O = 20mA$ | | | 1.0 | |
| V_{OL} | Low level output voltage, V_O | | | | 0.6 | |
| I_{IN+} | Logic "1" input bias current | $V_{IN} = 5V$ | | 10 | 20 | μA |
| I_{IN-} | Logic "0" input bias current | $V_{IN} = 0V$ | | 1.0 | 2.0 | |
| I_{O+} | Output high short circuit pulse current | $V_O = 0V$, $V_{IN} = 5V$ with $PW < 10\mu s$ | 250 | 350 | | mA |
| I_{O-} | Output low short circuit pulsed current | $V_O = 15V$, $V_{IN} = 0V$ with $PW < 10\mu s$ | 500 | 650 | | |
| V_S | Allowable negative V_S pin voltage for HIN signal propagation to HO | | | -9.8 | -7.0 | V |

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15.0V, $V_S = COM$, $C_L = 1000pF$, and $T_A = 25^\circ C$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------|-------------------------------------|-----------------------------------|------|------|------|------|
| t_{on} | Turn-on propagation delay | $V_S = 0V$ | 100 | 170 | 300 | ns |
| t_{off} | Turn-off propagation delay | $V_S = 0V$ or 200V ⁽⁵⁾ | 100 | 200 | 300 | |
| t_r | Turn-on rise time | | 20 | 60 | 140 | |
| t_f | Turn-off fall time | | | 30 | 80 | |
| MT | Delay matching, HS & LS turn-on/off | | | | 50 | |

Note:

5. This parameter guaranteed by design.

Typical Characteristics

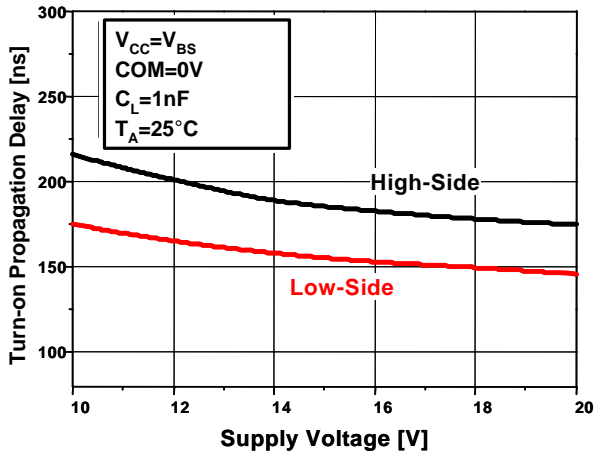


Figure 4. Turn-On Propagation Delay vs. Supply Voltage

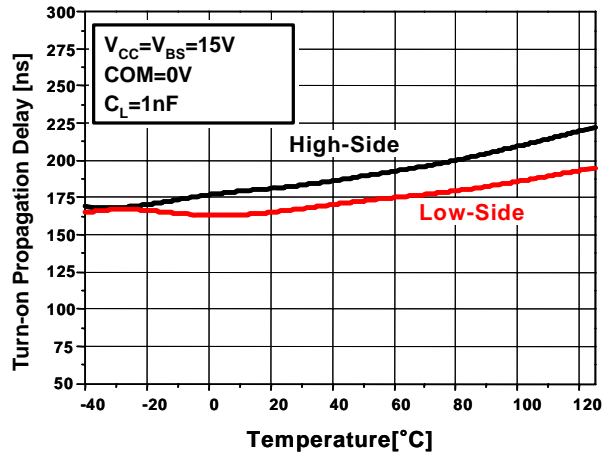


Figure 5. Turn-On Propagation Delay vs. Temp.

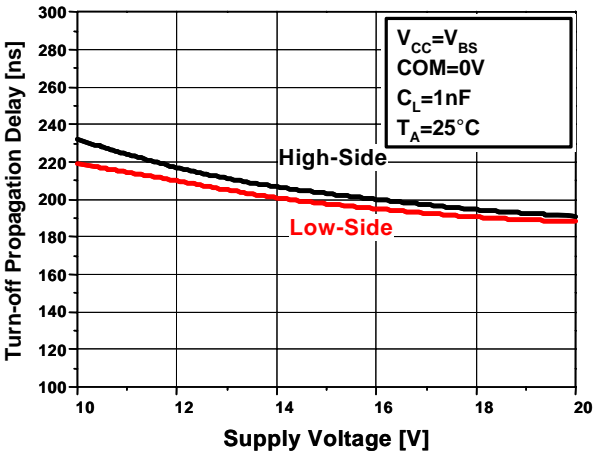


Figure 6. Turn-Off Propagation Delay vs. Supply Voltage

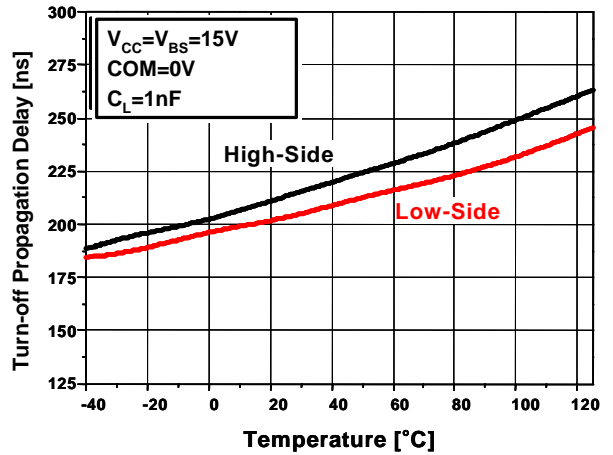


Figure 7. Turn-Off Propagation Delay vs. Temp.

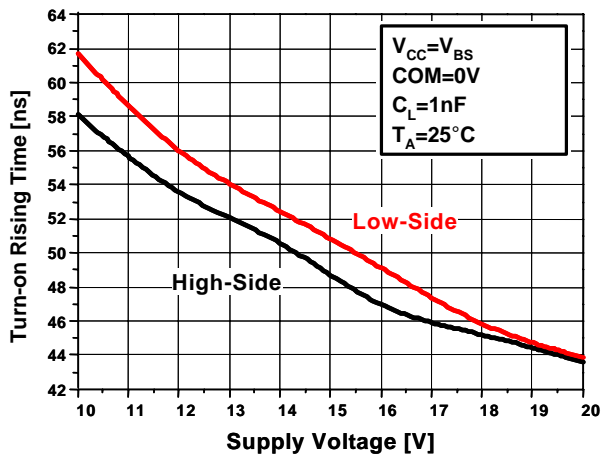


Figure 8. Turn-On Rising Time vs. Supply Voltage

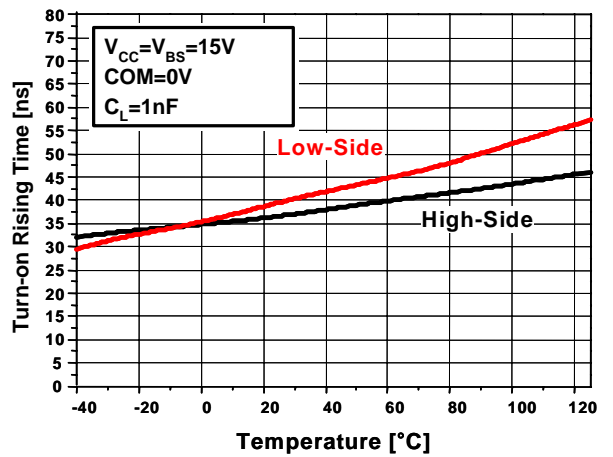


Figure 9. Turn-On Rising Time vs. Temp.

Typical Characteristics (Continued)

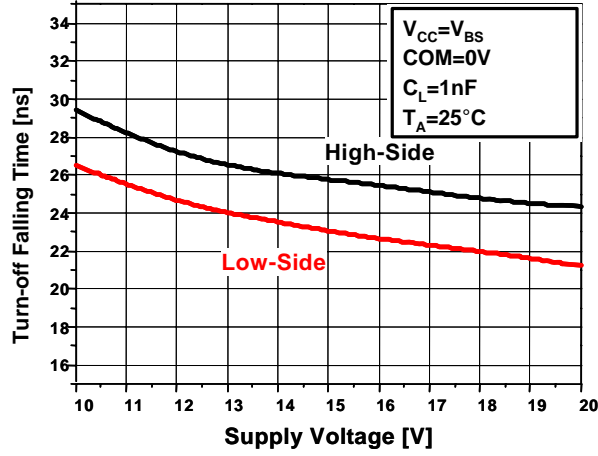


Figure 10. Turn-Off Falling Time vs. Supply Voltage

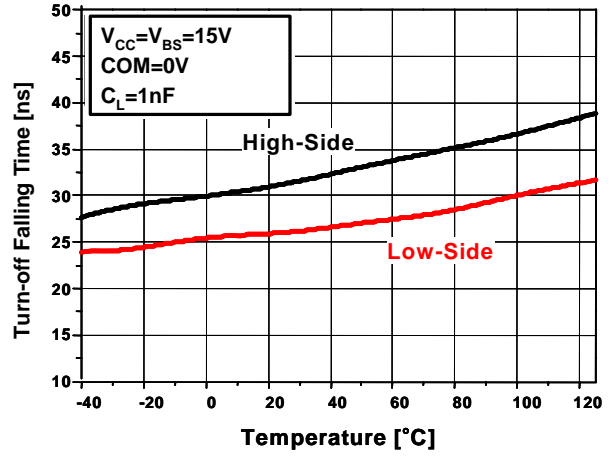


Figure 11. Turn-Off Falling Time vs. Temp.

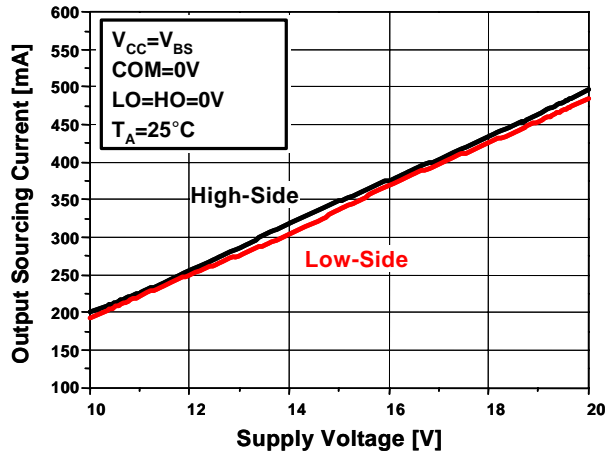


Figure 12. Output Sourcing Current vs. Supply Voltage

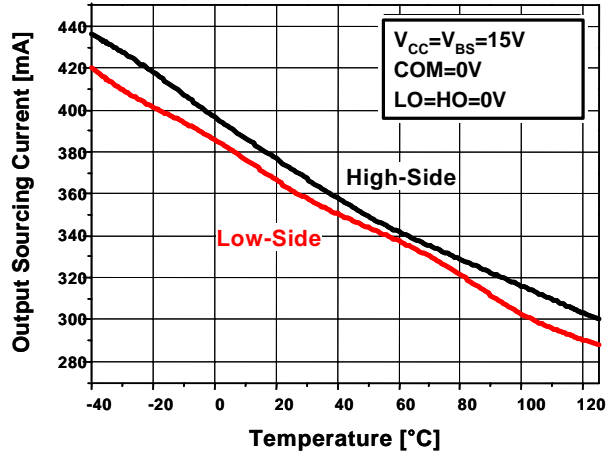


Figure 13. Output Sourcing Current vs. Temp.

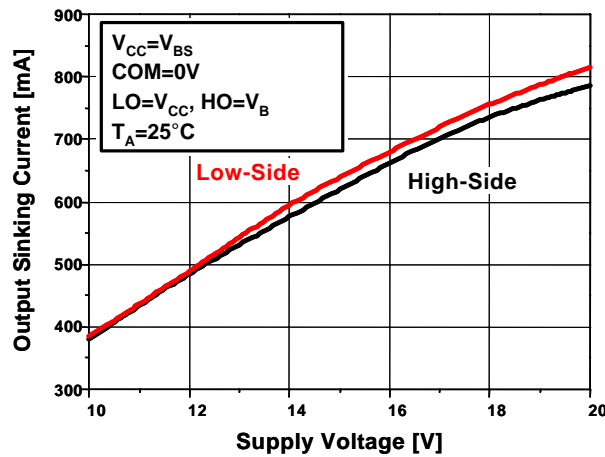


Figure 14. Output Sinking Current vs. Temp.

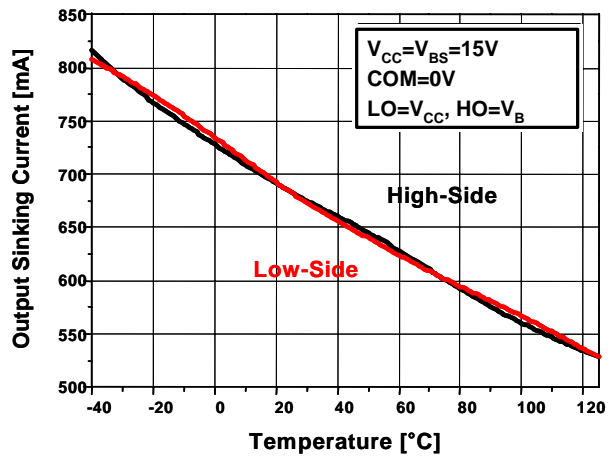


Figure 15. Output Sinking Current vs. Temp.

Typical Characteristics (Continued)

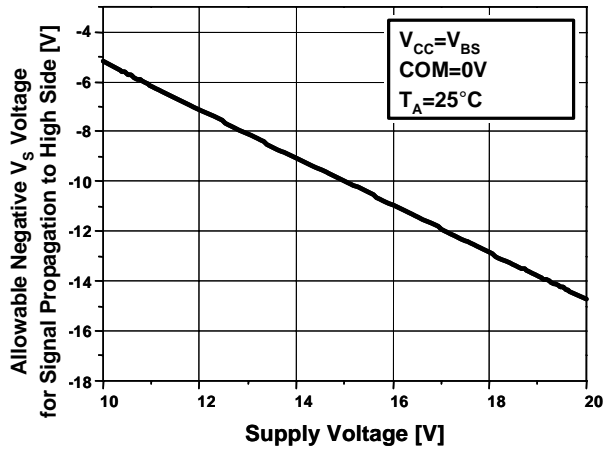


Figure 16. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Supply Voltage

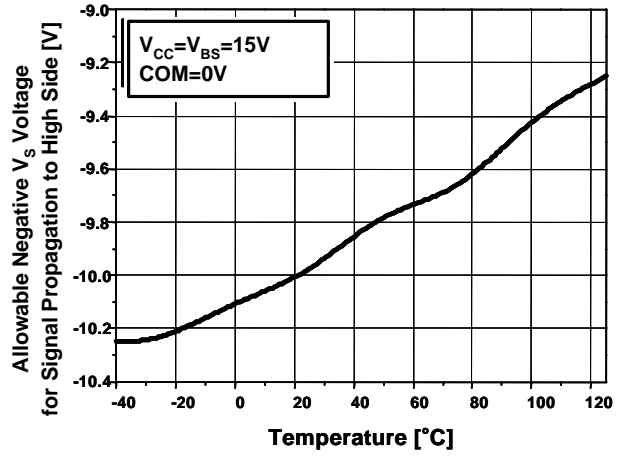


Figure 17. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Temp.

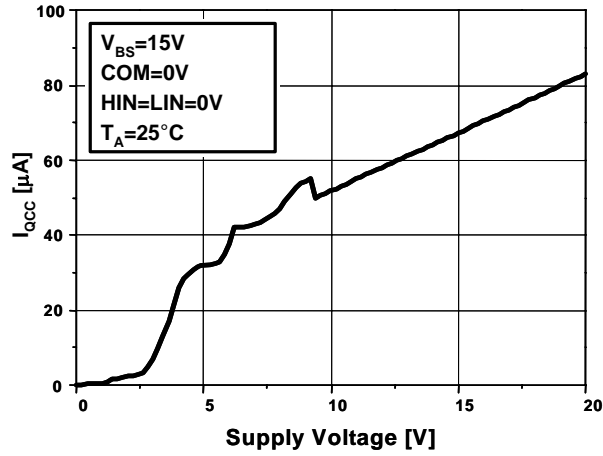


Figure 18. I_{QCC} vs. Supply Voltage

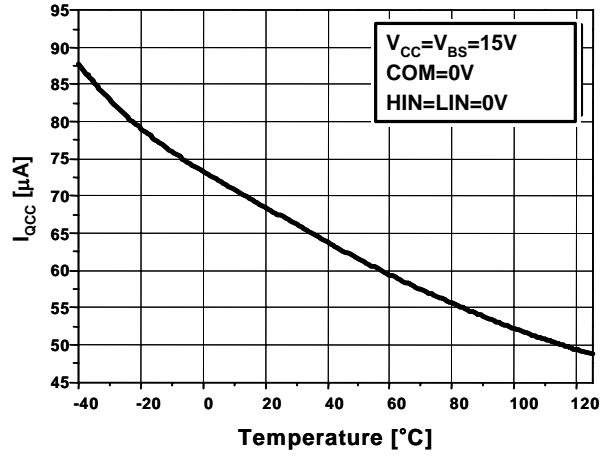


Figure 19. I_{QCC} vs. Temp.

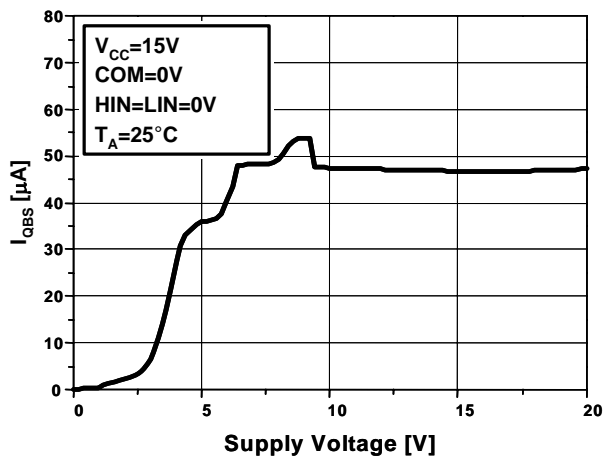


Figure 20. I_{QBS} vs. Supply Voltage

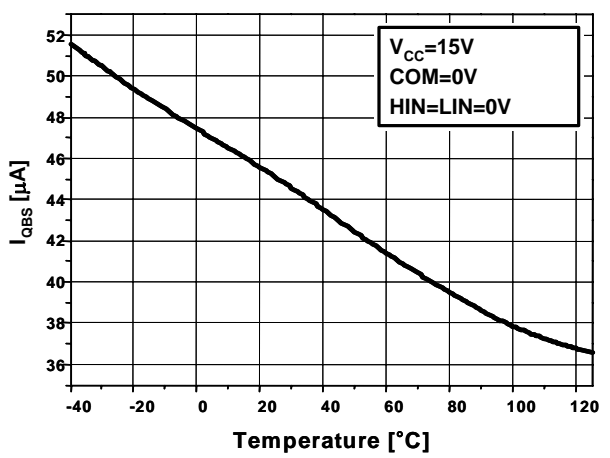


Figure 21. I_{QBS} vs. Temp.

Typical Characteristics (Continued)

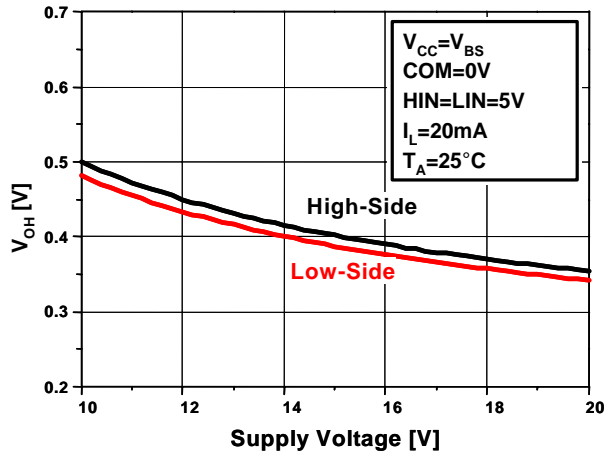


Figure 22. High Level Output Voltage vs. Supply Voltage

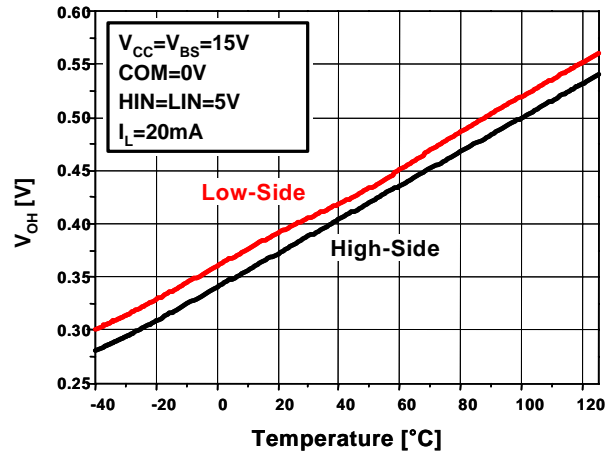


Figure 23. High Level Output Voltage vs. Temp.

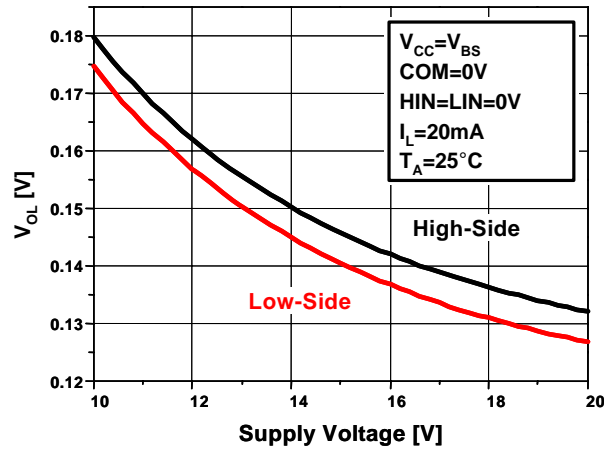


Figure 24. Low Level Output Voltage vs. Supply Voltage

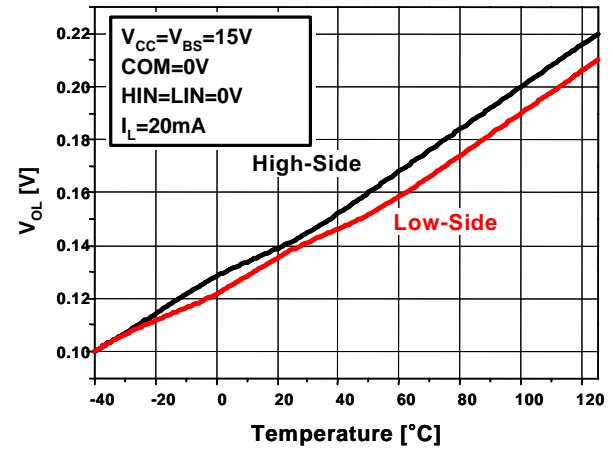


Figure 25. Low Level Output Voltage vs. Temp.

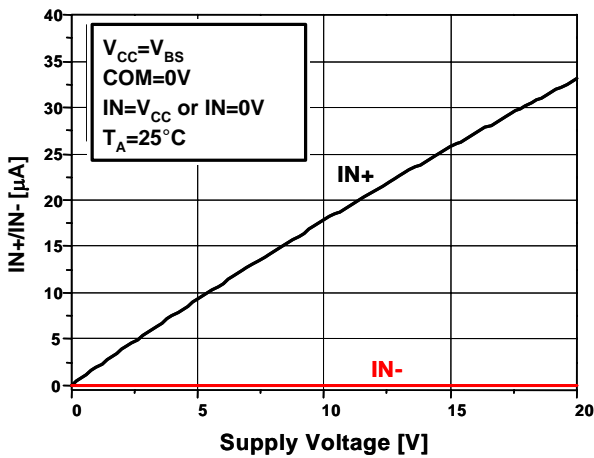


Figure 26. Input Bias Current vs. Supply Voltage

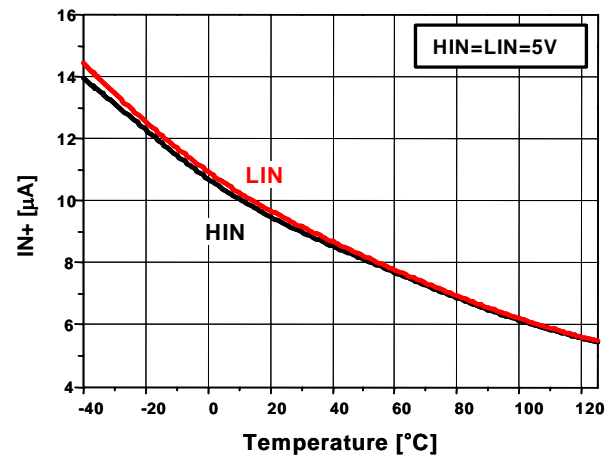


Figure 27. Input Bias Current vs. Temp.

Typical Characteristics (Continued)

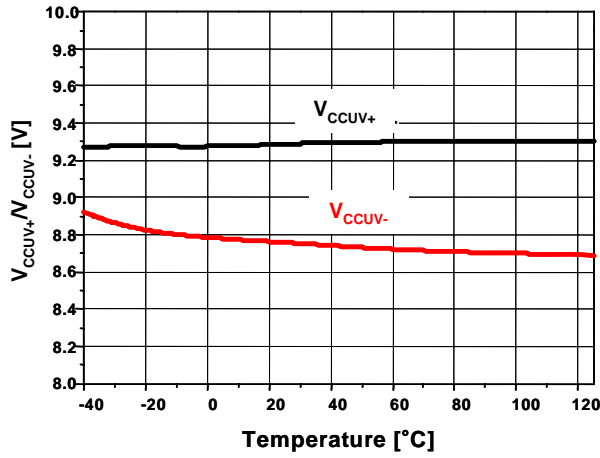


Figure 28. V_{CC} UVLO Threshold Voltage vs. Temp.

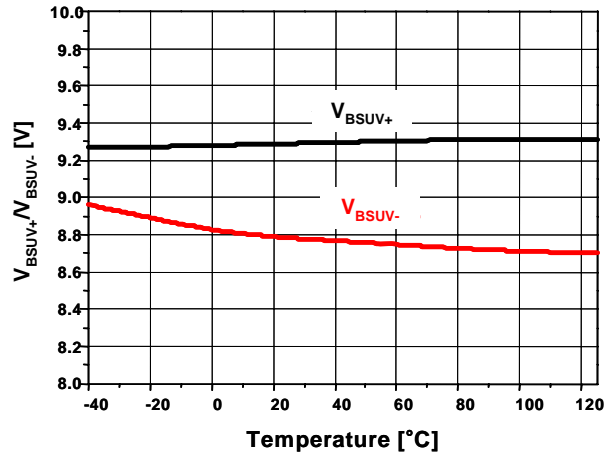


Figure 29. V_{BS} UVLO Threshold Voltage vs. Temp.

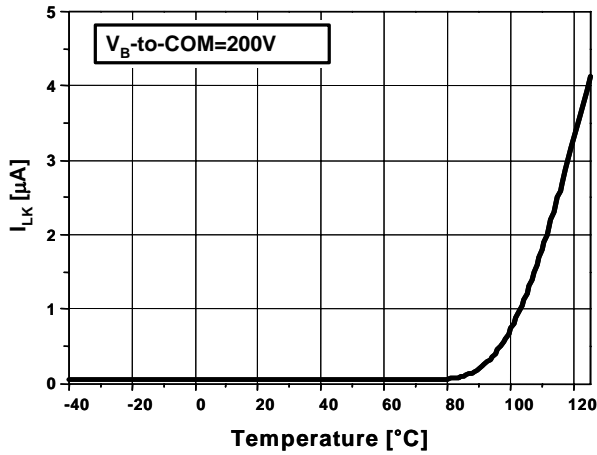


Figure 30. V_B to COM Leakage Current vs. Temp.

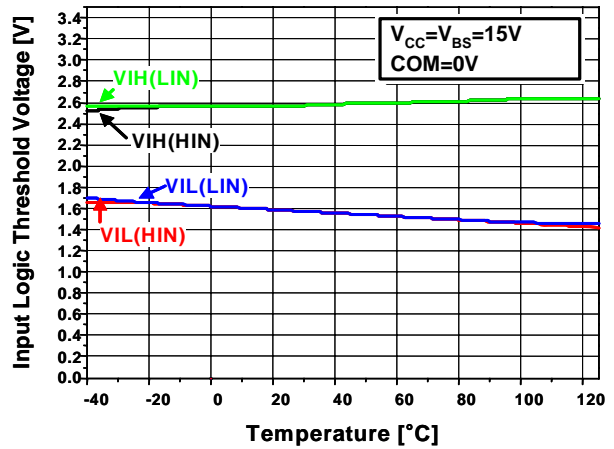


Figure 31. Input Logic Threshold Voltage vs. Temp.

Applications Information

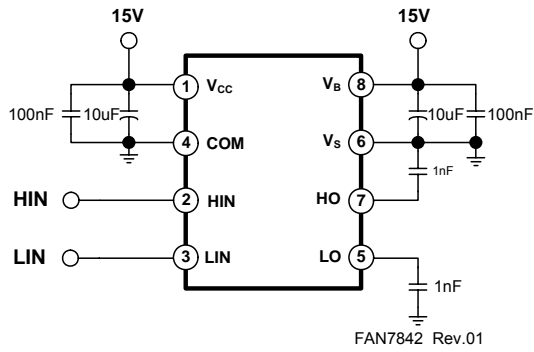


Figure 32. Switching Time Test Circuit

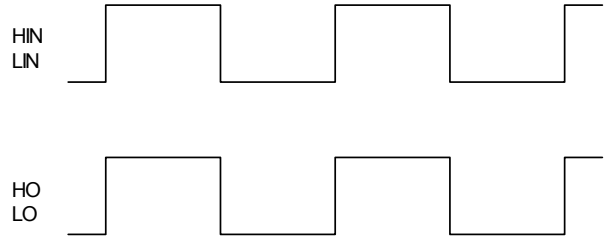


Figure 33. Input / Output Timing Diagram

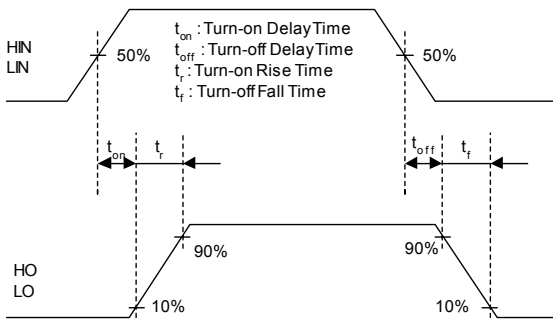


Figure 34. Switching Time Waveform Definitions

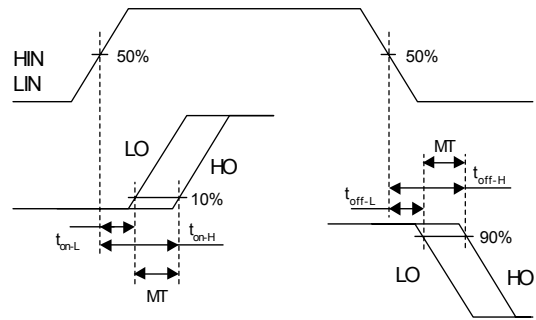
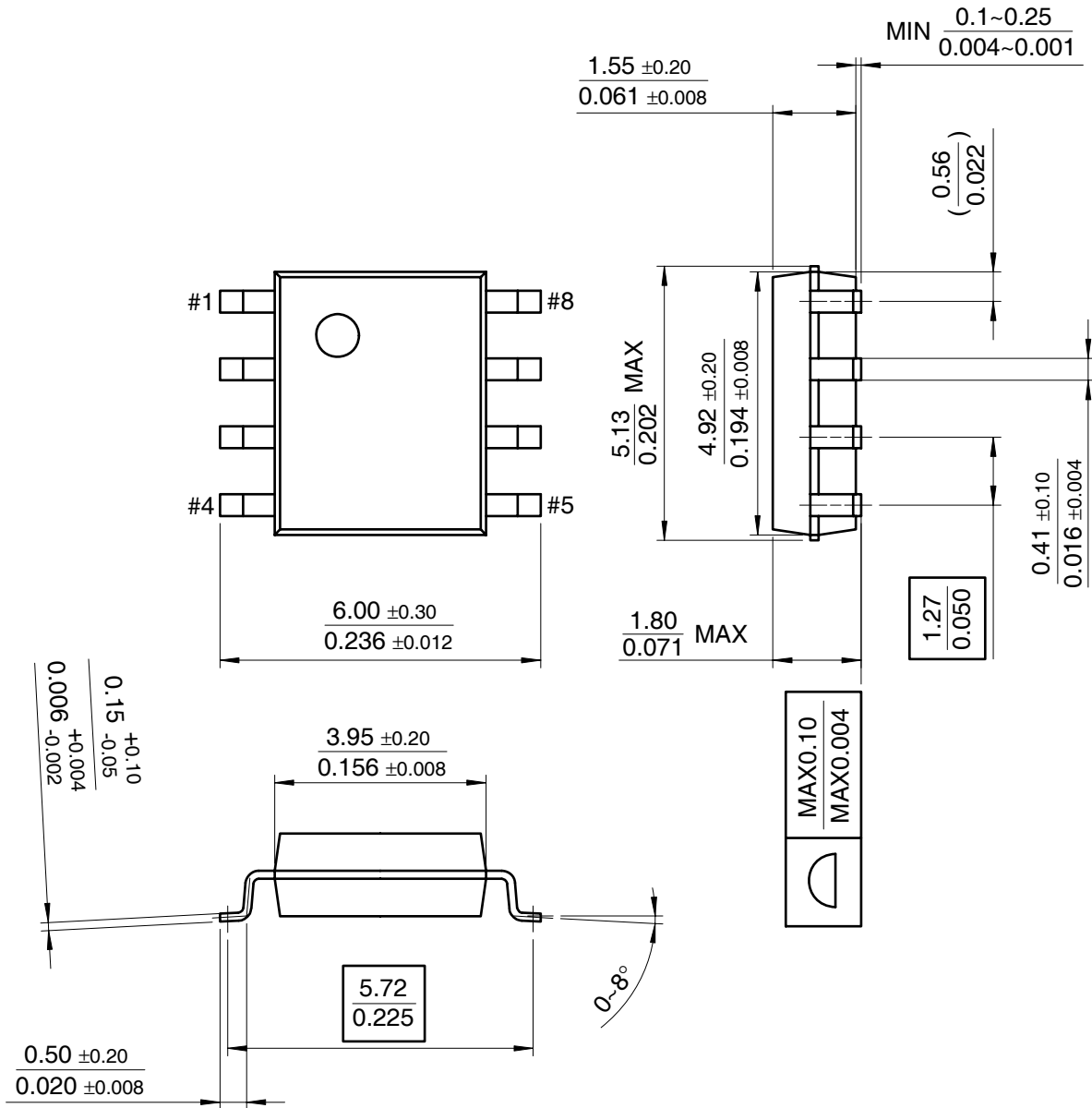


Figure 35. Delay Matching Waveform Definition

Package Dimensions

8-SOP

Dimensions are in millimeters unless otherwise noted.




September 2001, Rev B1
sop8_dim.pdf

Figure 36. 8-Lead Small Outline Package (SOP)



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